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(54) Communication system, a station to be used in such a system, and a gate connecting element to be used in such a system, as well as a device comprising such a gate connecting element.

(57) A communication system is described comprising different buses (20, 46, 56) which are interconnected via one or more gate connecting elements (20, 50). There is a transmitter station transmitting a frame that comprises a target address field and one or more destination address fields. If the send and receiver stations (46, 48, 52, 54) are connected to the same bus, the contents of the target address field are sufficient to define the receiver station. In other cases the target address field defines a gate connecting element, whereas the latter fills the the target address field with the contents of one of the other fields. In this way receiver station addresses, which have already been defined on a previous bus, can again be used on the next bus. Furthermore, in a short-frame format, receiver stations on the same bus as the transmitter station can be addressed with very low overhead.

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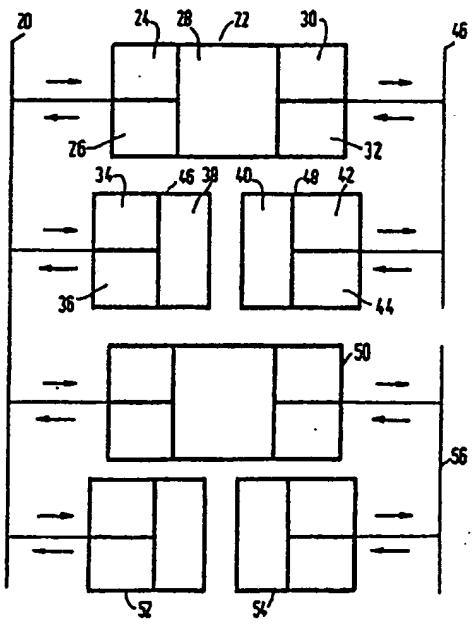


FIG.1

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Communication system, a station to be used in such a system, and a gate connecting element to be used in such a system, as well as a device comprising such a gate connecting element.

FIELD OF THE INVENTION.

The invention relates to a communication system on the basis of frames, to which communication bus system are connected a transmitter station, and a receiver station which is defined by a destination address. Such a system is used, for example, in a home for communicating control signals, and the organisation is such that the cost of the system and the cost of exploitation of the system remains low. Owing to the organisation on the basis of frames, a plurality of stations can alternately communicate with one another; basically, with each new frame a new combination of send and receiver stations can be formed. The transmitter station is, for example, a controlling microcomputer. The receiver station can be an apparatus for consumer entertainment, a domestic appliance (clock, microwave oven, washing machine), a sensor (temperature, security), a switch (light switch, a door switch or a control valve), or a station for communication with the outside world (modem, telephone answering machine). The address field in such a local communication bus system comprises a fixed number of bit positions, for example 8, so that a maximum of 256 objects can be indicated. In specific cases this number is insufficient. A larger length of the destination address field could be defined. In this case, owing to the frame organisation on the basis of bytes, the address length would immediately become twice as long, causing a frame to become 8 bits longer. For a frame comprising many bytes this would be only a relatively limited disadvantage. However, for the above switches and further simple stations a smallest possible frame length is usually aimed at, so that an extension by 8 bits would be a relatively large disadvantage indeed as the overhead will become much larger then. A further disadvantage of extending the destination address is the fact that all stations would have to include a complicated address decoder.

EXEMPLARY BACKGROUND ART

A particular example of such a multi-station network with multiple buses has been described in European Patent Application 60535, corresponding to United States Application Serial No. 243,013, filed March 12, 1982 to Recognition Equipment Corporation. The problem addressed by this citation is to relieve the various buses of the bus system from waiting for transport between stations connected to another bus. This is reached by introducing gate connection elements between buses as separately addressable items. If not addressed, the connection element remains closed. The known solution does not provide for an extendable address length that would be useful, both for locally addressing elementary stations and more complex stations, and for, across one or more such gate connection elements address any station, in the latter case also allowing for extendable data fields.

SUMMARY OF THE INVENTION.

Among other things, it is an object of the invention to improve the addressing facilities in a bus system mentioned in the opening paragraph to the effect that with a fixed address field length it is rendered possible to re-use an address already assigned within the address field, without creating ambiguous addressing, so that unintentional addressing is avoided, whilst retaining the possibility of defining a (very) small frame length under specific circumstances.

This is achieved, according to a first aspect of the invention, by means of a communication system comprising a bus system having a first bus and a second bus interconnected by a first gate connecting element, said communication system comprising a transmitter station connected to said first bus and a receiver station connected to any of said first and second bus, said transmitter station having a frame generator for generating a frame having at least a frame length indicator, an address and a data item, a first content of said frame length indicator specifying a short-frame format having a first fixed address length and a first fixed data item length that are exclusively operative on the same bus as the transmitter station is connected to, a second content of said frame length indicator specifying a long-frame format having a second fixed address length that is exclusively operative on the same bus as the transmitter station is connected to and a second specifyable data item length, said second fixed address length allowing for specifying either said receiver station by way of destination address when the receiver station is connected to the same bus as the transmitter station, or for specifying said first gate connection element by way of target address when the receiver station is connected to the second bus, said long-frame format in the latter case accommodating also said receiver station's destination address, said first gate connecting element including trans-

posing means for then transposing the destination address field's content to the target address' field, as a result of which the receiver station can be addressed directly when the above frame is transmitted over the second bus.

Short frames can now be used with a similar bus, whereas only limited intelligence needs to be incorporated in a gate connecting element. If it is assumed that the destination station is a video recorder, the station can be connected both to the first bus, addressed only by the destination address, and the second bus, addressed by the combination of target address and destination address. Alternatively, it is possible to use two video recorders having identical addresses and being connected to the first and second bus respectively. These addresses are often determined by the internal hardware of the receiver stations and thus no change of this hardware will be required. Transmitter stations addressing a receiver station over the same bus need not be modified either. For example, a television receiver may address a dedicated video recorder in an unmodified fashion. Only when a transmitter station intends to address a receiver station over a different bus viaa gate connecting element, must the relevant frame comprise both the target address and the destination address. However, such transmitter stations are usually software-programmable as is the case, for example, with a home computer or a control device for controlling light and indoor climate; in a case like that, setting the target address is simple.

FURTHER ASPECTS OF THE INVENTION.

The number of buses may be larger, with one or a plurality of gate connecting elements being inserted each time between two interconnected buses. In a case like this, various strategies with respect to transposing are possible. It is advantageous if the destination address field, as a first field, forms part of a series of various fields whose lengths have been preset, which series is situated between this first field and a last field, and said transposing means comprise rotating means for moving the contents of the remaining fields of the said series by one position in the direction of the first field in conjunction with said transposing operation, as a result of which said first field comprises a then current destination address, and further means for transposing the contents of the received target address field to said last field. Owing to this rotation it will be clear at the destination station which route the frame has followed. It will then be simple to return an acknowledge signal along the same route. The transmitter station will then write its own address in said last field. This need not necessarily be the last physical field of the series. Also the original address can be incorporated in this rotation.

Specific destination addresses can be permanently assigned to a specific category of stations, such as video recorders, thermostats or motion detectors for burglar alarms. A plurality of address contents are preferably reserved for gate connecting elements, so that for each bus various address contents can be specified by a respective target address. This enables a flexible configuration. For example, to each bus one video recorder can be connected which is addressable by the same destination address and respective contents of the target address field. It is likewise possible that two or more video recorders of this type are connected per bus, so that there are two (or more) possibilities for the contents of the destination address.

The invention likewise relates to a transmitter station and a gate connecting element to be used in a communication bus system in accordance with the invention. The invention also relates to a device, comprising a gate connecting element as stated hereinbefore, as well as at least two external connections for as many buses, and an internal station which is inserted between a user function in this device and at least one of the latter buses. For a consumer this simplifies the structure of such a communication system, because the gate connecting elements have become invisible as it were, and, consequently, the actual connecting instructions have become more simple.

Further attractive aspects are set out in sub-Claims.

BRIEF DESCRIPTION OF THE DRAWINGS.

The invention will now be further explained with reference to the following Figures, in which:

Fig. 1 shows a diagram of a communication bus system;

Fig. 2 represents a short-frame format;

Fig. 3 represents a long-frame format;

Fig. 4 is a block diagram of a device comprising a gate connecting element;

Table 1 illustrates a routing operation.

DESCRIPTION OF A PREFERRED EMBODIMENT.

Fig. 1 is a block diagram of a communication system according to the invention. It comprises three buses 20, 46, 56. The serial buses (1 bit wide) can be designed according to different technologies, such as coax, twisted pair or optical technology. There are two gate connecting elements 22, 50. There are four further stations 48, 48, 52

and 54. With an 8-bit address length the number of stations per bus may vary from 0, 1... to a maximum of 256, including the gate connecting elements coupled to that bus. For a useful communication the number of non-gate-connecting-element stations connected to any bus usually is at least equal to two. The network structure may be different: wider buses, more buses, more stations, more gate connecting elements. A plurality of gate connecting elements may be interconnected between one pair of buses. The gate connecting elements themselves may even be interconnected to form an array-type structure. The buses may be realised in mutually different technologies; in that case, the relevant gate connecting elements are to comprise a technology converting mechanism, for example, between a coaxial cable, a twisted pair cable, an infrared connection or a glass fibre connection. The buses may also be organized according to different protocols, which difference may be manifested at different levels, such as the physical magnitudes (voltage, time), the bit format (NRZ, NRZ-1 and many others), the word format and higher levels. In that case the gate connecting element is to comprise a protocol converter. For simplicity such conversions are disregarded. All stations in this example operate bidirectionally. For example, station 46 comprises a transmitter device 36, a receiver device 34 and a data processor 38. Station 48 comprises a transmitter device 42, a receiver device 44 and a data processor 40. Gate connecting element 22 comprises transmitter devices 26, 30, receiver devices 24, 32 and data processor 28. In practice any connection to the bus will be bidirectional. Basically, it is possible for a station of a very simple structure to operate only as a receiver station and not even to send back an acknowledge signal. Generally, the stations can be very simple or more complicated. The width of the bus data path can be larger, for example 8 bits.

DESCRIPTION OF SEVERAL EXEMPLARY FRAME FORMATS

Fig. 2 shows an exemplary short-frame format. It can be used for controlling a simple station, for example, a switch. The frame counts 16 bits. The bits b0 ... b7 form the priority group. The value of the bits b2, b3, b4 is (011): this defines the frame format. The remaining bits b0, b1, b5, b6, b7 determine the priority level of the relevant frame. Basically, the priority can be determined by the nature of the communication, the identity of the transmitter station and the identity of the receiver station. If two or more prospective transmitter stations simultaneously commence a send operation, one station is selected by means of arbitration known per se, so that the station having the lower frame priority detects the multiplicity and withdraws. This occurs, for example, because the bus forms a wired AND-function: each logic -0- masks in that case any coincident logic -1-signals. The meaning of the remaining bits can be related to the identity of the transmitter station or the nature of the communication to be transmitted. The bits a0...a5 form a destination address field. Consequently, a maximum of 64 simple stations connected to the same bus can be addressed. If the arbitration by means of the priority group is ambiguous, the arbitration may be proceeded with the destination address bits. Bits c0, c1 define a simple command which may be formed in an appropriate and possibly unique manner for the relevant receiver station. For a switch this may be, for example: switch on, switch off, switch over, read the switch position. Basically, it is possible for two transmitter stations to apply exactly the same command to a single receiver station simultaneously. This is actually no objection.

Fig. 3 shows an exemplary format of a long frame. It is formed by means of a sequence of 8-bit bytes which are each indicated by a letter combination. Byte PR comprises the priority code wherein the bits b2, ... b4 naturally have a different value than < 011 >. Byte SA comprises the send address or original address. This can be used by the receiver station as a destination address for returning an ackowledge signal. For each bus this destination address is sufficient to unambiguously define a receiver station. For a specific physical station the destination address is invariant to the bus (20, 46, 56) to which the station concerned is actually connected. Byte CC comprises a verification code. At bit positions b0 ... b2, defined with respect to Fig. 2, this byte indicates the number of routing address positions. The remaining bit positions of byte CC are irrelevant here. Byte BC comprises the frame length code which may specify a length from 1 ... 256 bytes. The routing addresses are contained in bytes (RA1 ...RA7), if present. The quantity of these addresses is specified by byte CC. Thus, if the code in CC shows -0-, there is not a single routing address. The maximum number of routing addresses is 7 in this case. The first routing address is transposed to the position of the target address field DA in the first gate connecting element reaching the frame concerned. During this operation the contents of the fields SA, DA, RA1, RA2 ... RA7 are rotated as follows: DA, RA1, RA2 ... RA7, SA. After the second gate connecting element is reached, the sequence is again rotated by one position: RA1, RA2 ... RA7, SA, DA.

Finally, after at most seven gate connecting elements, the intended receiver station is reached. If the receiver station is reached at an earlier in-

stant, the unused routing addresses are omitted. In the latter case the last relevant gate connecting element shows, for example: RA5, SA, DA, RA1 ... RA4. In this case - target address - stands for the address determining the transport over the current bus, the destination address the address determining the transport over the next bus.

In another embodiment of the invention the original address sequence remains stationary; the series of routing addresses first comprises the target address DA, then the "real" routing addresses insofar as they are relevant. For the first bus transport the address DA is copied in the target address field, for the second bus transport the address RA1, for the third bus transport the address RA2 and so on, until the intended receiver station is reached. The address to be copied is indicated by bits in the byte CC. The remaining bytes of the frame are only referred to by way of illustration: byte HD provides a header, for example, a serial number or a code indicating that now the message proper commences. Byte SFA provides a source function address specifying the function of the source by means of an address for a local memory (in the definite receiver station). Byte DFA does the same for the function of the ultimate receiver station. Byte CD specifies a data unit or a command. Byte TC specifies a terminal code. Thus, it is possible for various CD bytes to be consecutive. Then a new header may appear. The frame end is specified by the contents of the byte BC. By counting down, the receiver station knows when this end occurs.

EXEMPLARY EMBODIMENT OF A DEVICE COMPRISING A GATE CONNECTING ELEMENT.

Fig. 4 is a block diagram of a device comprising a gate connecting element. Block 100 comprises a transceiver device to be connected to a single wire bus symbolized by connection 80. A receiver amplifier 82 feeding a signal comparator 86 as well as a shift register 90 are coupled to this connection 80. A series output of shift register 90 is connected to transmitter amplifier 84 and also to comparator 86. The transmitter amplifier is also connected to the bus. In the receive position, shift register 90 is serially loaded. In the send position, shift register 90 is read in series. If, in the latter case, the comparator 86 detects a discrepancy, this implies that the transmitted signal looses an arbitration and the relevant station, in this case the gate connecting element, is to stop transmitting. This is signalled to a local controller 102: transmission is terminated and possibly resumed at an instant to be determined later. Such mechanisms are known per se and are not further discussed for simplicity. Element 88 is a detector. It can in the first place detect the bits indicating a short-frame; if these bits are received the gate connecting element is deactivated. The bits of the priority byte are then only used for settling the arbitration between the prospective transmitter stations. If no short frame is concerned, the byte PR is stored in data RAM 96 by data register 94. In specific cases when the frame is transported, the gate connecting element generates its own individual priority byte and deactivates the received priority byte which is thus superseded. After the byte PR the byte SA is received. The latter is transferred to data register 94 via bus 92. Then the byte DA, the target address, is received. This byte is compared in comparator 98 to the relevant address of the gate connecting element. If the two match, there is an OK signal on line 104 to the local microprocessor 106 which, by means of address counter 108, stores the consecutive bytes on the respective positions of data RAM 96. During this operation bytes CC and BC have specific functions as has been mentioned hereinbefore: byte BC loads a down-counter and indicates, when the "0" count is reached, that the frame has been received completely. This counter is connected to bus 92 and not shown for simplicity. The byte CC comprises the indication over the number of routing addresses. They are loaded in register 110 (three bits). Thereafter, the remaining bytes of the frame are stored.

Similarly, there is a second transceiver device 98 which corresponds with device 100 and is therefore shown only in a notional fashion. The bus connection concerned is 112. The microprocessor 106 may be a conventional building block which, however, is programmed in a special way. If the addresses in the memory 96 range from 0...255, and the number of routing addresses range from 0...7, the addresses after being transposed are read according to Table 1. The first line shows the order in which the bytes are written. The second line shows the order in which they are read if a single routing address, the ultimate destination address, is present. In that case RA1(5) is read at position 2 and DA (target address) at position 1, and source address SA(1) at position 5. If there are two routing addresses, SA is read at position 7 and so on, up to, eventually, position 11, if there are 7 routing addresses. The addresses are supplied by the controller 108 of the microprocessor 106 which is connected to the register 110.

In the case under discussion the microprocessor 106 comprises not more than a single bus 92 for data and addresses. In many cases there are two separate buses. For simplicity this is not further discussed: in that case there will generally be in excess of 8 address bits. The memory 96 can

then, for example, accommodate two frames which are received simultaneously (more or less) at terminals 80, 112. The memory 96 can then accommodate further user information, for example, if the relevant gate connecting element forms part of a controller which transmits preset control frames to respective stations at specific instants. For this purpose, the local device may also comprise user input/output equipment 114 such as a keyboard and a screen. In this case the station function is integrated to a large extent with that of the gate connecting element. In another embodiment of the invention the user function comprises an individual transceiver device (100, 98) on one of the two bus terminals. Different arrangements such as may be present have not been indicated separately for simplicity:

- physical conversion between the signals at terminals 80,112 (LR/twisted pair/coax)
- ditto protocol conversion
- separate data processing in the user's function
- detailed structure of the microprocessor of the gate connecting element.

Claims

1. A communication system comprising a bus system having a first bus and a second bus interconnected by a first gate connecting element, said communication system comprising a transmitter station connected to said first bus and a receiver station connected to any of said first and second bus, said transmitter station having a frame generator for generating a frame having at least a frame length indicator, an address and a data item, a first content of said frame length indicator specifying a short-frame format having a first fixed address length and a first fixed data item length that are exclusively operative on the same bus as the transmitter station is connected to, a second content of said frame length indicator specifying a long-frame format having a second fixed address length that is exclusively operative on the same bus as the transmitter station is connected to and a second specifyable data item length, said second fixed address length allowing for specifying either said receiver station by way of destination address when the receiver station is connected to the same bus as the transmitter station, or for specifying said first gate connection element by way of target address when the receiver station is connected to the second bus, said long-frame format in the latter case accommodating also said receiver station's destination address, said first gate connecting element including transposing means for then transposing the destination address field's content to the target address' field, as a result of which the receiver station can be addressed directly when the above frame is transmitted over the second bus.

2. A communication system as claimed in Claim 1, wherein the first gate connecting element acts as a transmitter station for a second gate connection element that is connected to the second bus for thereon acting as a receiver station, and which is, together with a second receiver station, is connected to a third bus.

3. A communication system as claimed in Claim 2, comprising a series of interconnected buses, wherein respective gate connecting elements are inserted between any pair of interconnected buses.

4. A communication system as claimed in Claim 1, 2 or 3, wherein two receiver stations having identical destination addresses are connected to different buses of the system and can be addressed by a specific transmitter station by means of identical destination addresses and different target addresses.

5. A communication system as claimed in one of the Claims 1 to 4, wherein the destination address field, as a first field, forms part of a series of various fields of uniform lengths, which series is situated between this first field and a last field, and said transposing means comprise rotating means for moving the contents of the remaining fields of said series by one position in the direction of the first field, in conjunction with the said transposing operation, as a result of which said first field comprises a then current destination address, and further means for transposing the contents of the received target address field to the said last field.

6. A communication system as claimed in Claim 5, wherein the transmitter station further includes an original address generator for filling said last field with an original address, so that the frame in this last field always indicates the current origin on that bus.

7. A communication system as claimed in one of the Claims 1 to 6, wherein said receiver station is included in a category of stations, and the contents of the destination address formed by the transmitter station are permanently assigned to said category.

8. A communication system as claimed in one of the Claims 1 to 7, wherein each one of a plurality of gate connecting elements connected to an arbitrary bus can be defined by individual contents of the target address field.

9. A communication system as claimed in one of the Claims 1 to 8, wherein all said buses comprise a data path having a width of 1 bit.

10. A communication system as claimed in any of claims 1 to 9, wherein said first fixed data item length is less than a lower bound to said second specifyable data item length.

11: A communication system as claimed in any of claims 1 to 10, wherein short-frame format has a length which is less than a second lower bound to said long-frame format's length.

12. A transmitter station for use in a communication system as claimed in one of the Claims 1 to 11, wherein the transmitter device is operative for placing said target address field in a frame position before any destination address field when a receiver station is to be activated which is connected to a different bus than the above transmitter station.

13. A gate connecting element for use in a communication system as claimed in one of the Claims 1 to 11, comprising a local memory for storing the contents of all said fields in order of their reception, and read control means for reading out, upon reception, the contents of the said destination address field in a time position which corresponds with a receive position of said target address field inside the frame.

14. A device comprising a gate connecting element as claimed in Claim 13, and also including at least two external connections for as many buses, and an internal station that is connected between a user function in that device and at least one of the latter buses.

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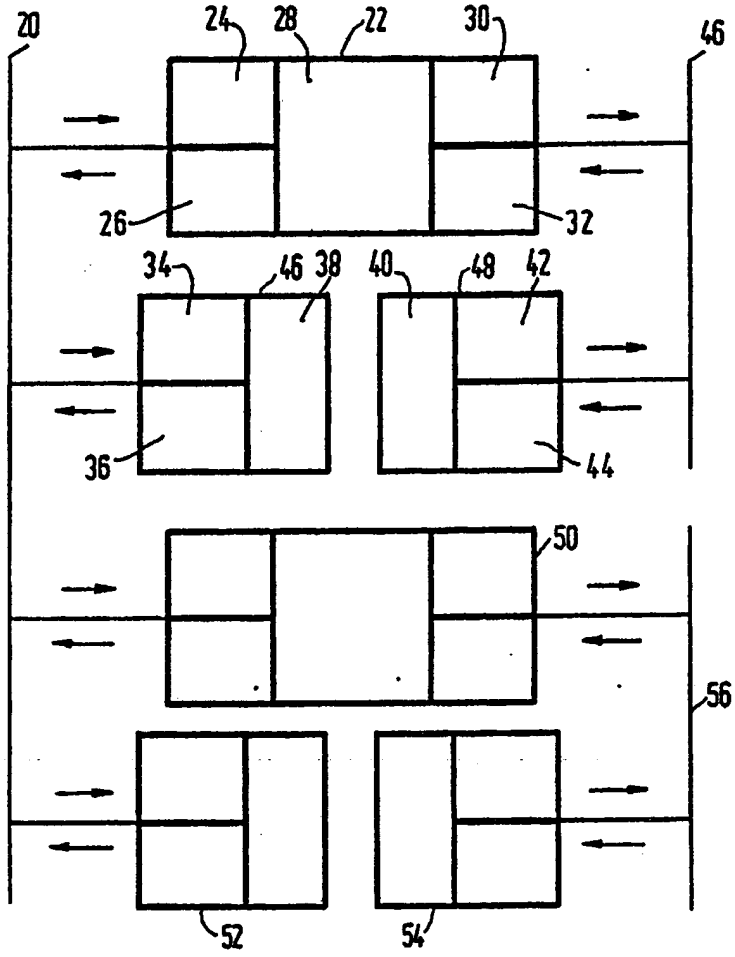


FIG.1

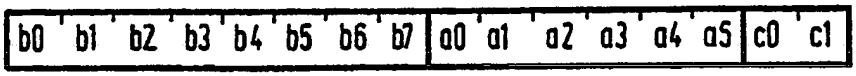


FIG.2



FIG.3

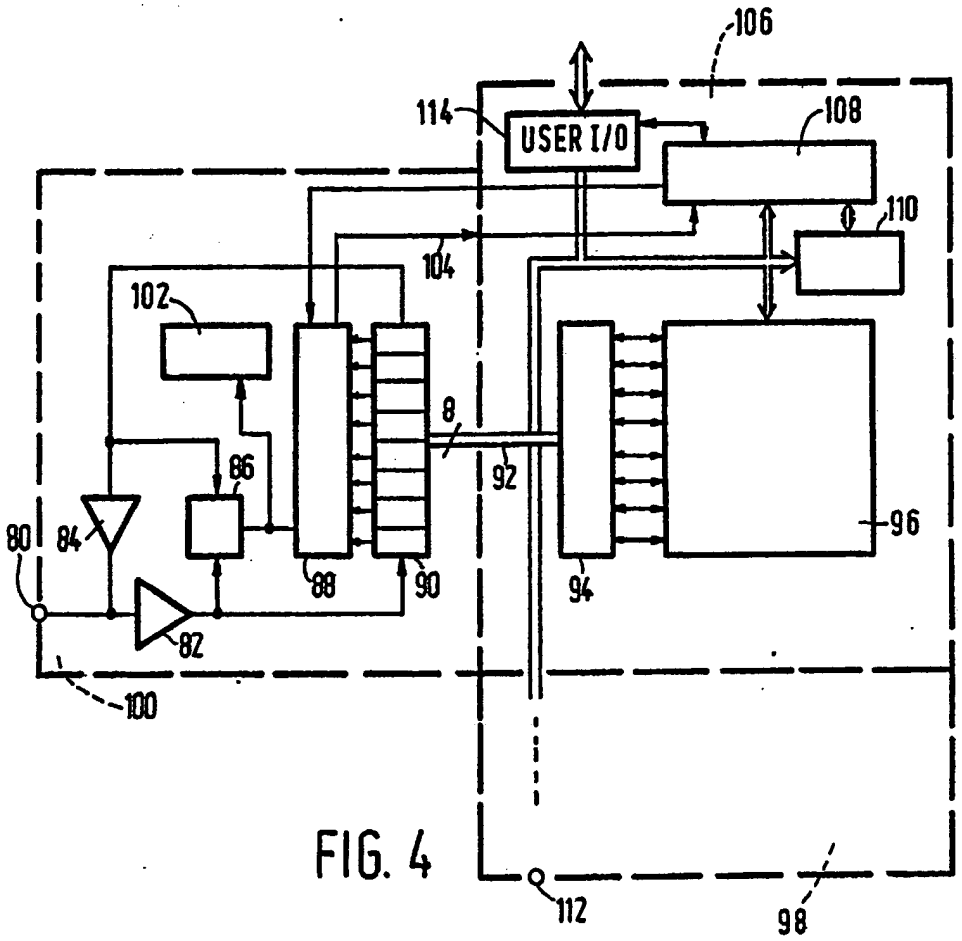


FIG. 4

In	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Out	0	2	5	3	4	1	6	7	8	9	10	11	12	13
	0	2	5	3	4	6	1	7	8	9	10	11	12	13
	0	2	5	3	4	6	7	1	8	9	10	11	12	13
	0	2	5	3	4	6	7	8	1	9	10	11	12	13
	0	2	5	3	4	6	7	8	9	1	10	11	12	13
	0	2	5	3	4	6	7	8	9	10	1	11	12	13
	0	2	5	3	4	6	7	8	9	10	11	1	12	13

TAB. 1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 89 20 2167

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 5)
A,D	EP-A-0 060 535 (REGOGNITION EQUIPMENT) * Page 4, lines 1-15; page 6, lines 1-15; page 7, line 15 - page 8, line 4; figures 1,2 *	1,12,13	H 04 L 12/46 G 08 C 15/00 G 06 F 13/40
A	EP-A-0 156 542 (INTERNATIONAL COMPUTERS) * Page 5, line 22 - page 6, line 26; page 12, lines 15-19; figures 1,4 *	1,2,3,9	
A	US-A-3 731 002 (PIERCE) * Column 3, line 37 - column 5, line 34; column 23, line 32 - column 24, line 50; figures 1,2A,2B,14A,15 *	1,5,6	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 26, no. 3A, August 1983, pages 1198-1200, New York, US; R.C. DIXON: "Group address structure for network service nodes" * Page 1198, line 1 - page 1200, line 15; figures 1-45 *	1,7,8	
A	DE-A-3 514 334 (SIEMENS) * Whole document *	1	TECHNICAL FIELDS SEARCHED (Int. Cl. 5) G 06 F G 08 C H 04 L
A	WO-A-8 706 379 (REGULEX) * Page 5, line 9 - page 8, line 4; page 13, line 34 - page 14, line 18; figures 1-3,7 *	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	11-10-1989	WANZEELE R.J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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